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The U.K. LINK Personal Communications Programme: Downlink Synchronisation for a DS-CDMA Field Trial System

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Abstract- DS-CDMA is recognised as one of the foremost radio access techniques today. However, to date, there has been relatively scant information on the system implementation and the many problems facing radio engineers. In this contribution, a DS-CDMA field trial demonstration system is described briefly, before discussing in detail the vital process of acquisition and synchronisation at the mobile and its practical implementation.

I. INTRODUCTION

The emergence of DS-CDMA as a viable air interface technique for current and future personal communications systems is the driving force behind many research and development initiatives worldwide. In the U.K., a collaborative research project was established early in 1992 with the specific intention of evaluating CDMA techniques for the future of mobile radio as embodied by the proposed European third-generation standard, referred to as the *Universal Mobile Telecommunications System* (UMTS), and the ITU *Future Public Land Mobile Telecommunications Systems* (FPLMTS) standard. The motivation for this work is to look beyond the range of current second-generation digital standards, both cordless and cellular, and to offer users unified radio access on an unprecedented universal scale. The aim is to provide a service which will, in effect, be a wireless extension of the rapidly developing fixed network, offering the equivalent quality and variety of services, e.g. toll quality speech, data, video and a host of multi-media applications.

Given these ambitious goals, extensive work is currently underway to facilitate the selection of the most suitable air interface, or interfaces. Current second-generation systems are almost exclusively TDMA, with a host of variants offered worldwide, e.g. DECT, GSM, DCS1800, DAMPS. However, this dominance has been challenged recently with the emergence of a rival CDMA standard in the U.S. [1]. Developed by Qualcomm, this revolutionary system has generated immense interest worldwide and, as a result, CDMA is also being considered as a candidate for the UMTS/FPLMTS standard. Given the significant advances required over second-generation systems, the technological challenges presented to both techniques are not trivial, especially given the increased data rates, flexibility and overall system capacity required. Consequently, there appears to be no particular advantage associated with either access method at this time. The RACE initiative in Europe has already tackled this problem with two projects set up to assess the feasibility of TDMA and CDMA [2]. They are known as ATDMA and CODIT, and with

the test beds due for completion in 1995, it is hoped that the comparative trials will yield the most viable solution.

The work in this paper is from a U.K. LINK project entitled "*A Rigorous Evaluation of CDMA for Third Generation Systems*". The work has been running for nearly three years and, although it initially considered both frequency-hopping (FH) and direct-sequence (DS) CDMA [4], has selected the latter to take forward and develop into a field trial demonstrator. Development of the field trial system is well underway, with extensive trials planned for 1995. The aims of these trials can be summarised as follows:

- To demonstrate a subset of the proposed UMTS services with a DS-CDMA air interface in a variety of cellular environments.
- To study and assess the performance of a number of key system issues relating to DS-CDMA, namely:
 - spreading at 8.192Mchips per second,
 - closed-loop power control at different rates,
 - macroscopic diversity, or soft handover, between two base-stations,
 - coherent Rake reception at both the base and mobile.
- To measure and predict system capacity through artificial cell loading.
- To improve the general understanding of a DS-CDMA system and the problems facing system and network designers in its implementation.

The field trial system, as illustrated in figure 1, will be the culmination of over three years' work and comprises two base-station (BS) and two mobile station (MS) units, connected together through the fixed network via a Mobility Manager (MM). It is planned to carry out the field trials in as broad a range of environments as possible, in line with current and proposed cell types. These include street-level micro-cells as well as the larger rooftop mounted macro-cells. Handover will also be demonstrated, with the BS's separated using a microwave link.

The aim of this paper is to present a brief overview of the design of the forward or downlink air interface [3], i.e. the interface from the base-station to the mobile, before focusing in greater detail on the crucial process of synchronisation in the mobile. This covers all the steps required to enable the mobile to establish an initial connection with a base-station prior to any call set-up being initiated. Details on the hardware design will be presented along with some implementation issues.

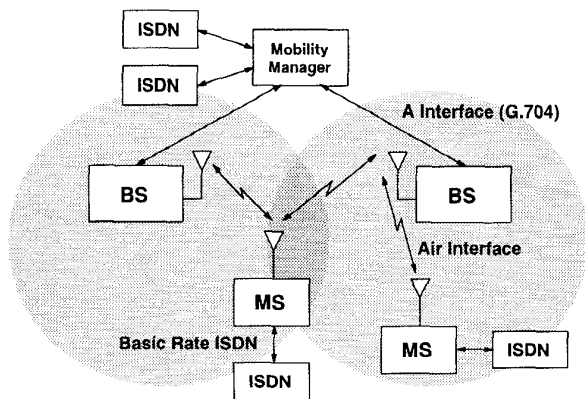


Figure 1: Field trial system architecture.

II. DOWNLINK DESIGN

A. Channel Structure

A number of channels have been defined to support the downlink air interface as follows:

Pilot Channel - PIC	Common System Channels
Sync Channel - SYC	
Power Control Channel - PCC	Dedicated User Channels
Forward Control Channel - FCC	
Forward Traffic Channel - FTC	

These are split between those common channels supported at each base-station and those allocated to each user. Each channel is assigned a separate PN code, as discussed in a subsequent section. Their attributes can be summarised as follows:

- **PIC** - This channel transmits no data other than a PN spreading sequence. This is essential to allow the MS to acquire and synchronise to the BS, as well as allowing coherent demodulation of the data channels and supporting diversity handover operation.
- **SYC** - This is a low rate (1kbps) continuous data channel which carries essential system information to allow the user to establish a connection with the network. This includes the BS identifier and system timing information.
- **PCC** - A variable rate continuous channel (≤ 4 kbps) to control the MS transmit power during a call. Available rates are: 0.25, 0.5, 1, 2 and 4kHz.
- **FCC** - This channel carries all the signalling and control messages required by the MS. This includes any paging access from the BS, as well as call control, etc. The channel is not continuous and supports a data rate of 64kbps.
- **FTC** - This channel carries only the continuous user data at a rate of 64kbps. Given the limited resources available to the project and the broad goals of UMTS, it was decided to target only a limited subset of services and environments which would rigorously stress the air interface. In order to further simplify the design and the interworking requirements, the

services, and in particular the bearer services, were mapped directly to ISDN and were designed around a basic 64kbps data rate. Two bearers have been selected for the field trial as defined in table 1. Bearer A will support 64kbps speech whilst bearer B will support a range of data services, e.g. Group 3 Fax, integrated voice and data as well as 64kbps data. Although both are at 64kbps, the architecture could be enhanced at a later date to support a 128kbps bearer.

	A	B
Throughput	64 kbps	64kbps
Error Rate	10^{-3}	10^{-6}
Delay (max.)	40msec	100msec
Delay Distribution	narrow	narrow
Occupancy	35%	100%

Table 1: Demonstration bearer services.

B. PN Code Assignment

Two distinct sets of PN sequences are required to support the above channel structure: short sequences for the system channels and longer sequences for the user channels. The short sequences for the PIC and SYC channels are to enable the MS to rapidly acquire and track the PN code. The chosen code was an augmented m-sequence, 2^{17} chips long, and at a chipping rate of 8.192Mbps, this gives a code repetition rate of 16msec. Code allocation is achieved by assigning different base-stations a unique time offset of the same code. The offset must be greater than the expected maximum excess delay in the channel to avoid incorrect channel estimates. Also, the code must be long enough to ensure sufficient separation between BS's before the same offset is re-used, but short enough to enable rapid code acquisition. An augmented sequence was selected to ensure an even length sequence since the Pilot is also employed to establish frame synchronisation. Note that in order to allow the same codes to be used at each BS, the sites must be closely synchronised. This is achieved by the mobility manager over the A interface.

The requirements for the long user codes are very different and the decision was based upon the need for a large set of codes with a sharp auto-correlation function and low cross-correlation to minimise interference from other users [5]. Orthogonal spreading was not considered to be applicable here due to the limited code set and the possible problem of supporting multiple bearer rates. The chosen strategy was to employ a single very long m-sequence with each user assigned a unique offset. This offset is determined by the users' unique ID number and, with a long enough code length, would offer effectively an unlimited code set and remove the need for code planning. The chosen length for the field trial system is $2^{29}-1$ chips long, which is a compromise between length and practical implementation issues. It is envisaged that any future commercial embodiment of this system would employ a significantly longer code.

C. Channel Coding & Modulation

The remaining key parameters for the downlink air interface can be summarised as follows:

- RF Carrier Frequency - 1823 MHz
- Chipping Rate (f_c) - 8.192Mbps
- Error Control Coding - $\frac{1}{2}$ rate, constraint length 7, convolutional code.

- Block Interleaving - 12msec frames for speech and 36msec frames for data.
- Modulation & Spreading - QPSK with a preferred pair of PN sequences.
- Pulse Shaping - 44 tap digital FIR filter (signal BW = 9.8MHz).

D. Mobile Receiver & Demodulator

A simplified breakdown of the mobile receiver and demodulator is given in figure 2. The received RF signal at 1823MHz is mixed down to a first IF at 70MHz. Here, AGC is carried out prior to the final downconversion process to baseband in quadrature and analogue-to-digital conversion. Thereafter follows the process of extracting the user data from the spread signal. Crucial to this whole process is the acquisition and tracking of the Pilot signal transmitted by the BS. This synchronisation process is on a number of levels and will form the focus for the rest of this paper. Details on the overall receiver and demodulator functions can be found elsewhere [4].

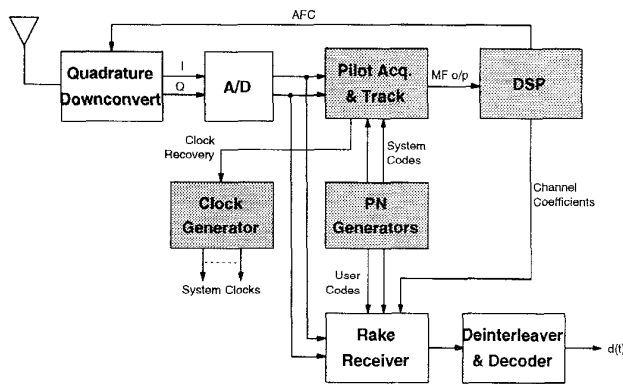


Figure 2: Receiver and demodulator structure.

III. PILOT ACQUISITION & TRACKING

The process of acquiring and tracking the Pilot is carried out continuously in the mobile and must support the following functions:

- Acquisition of the Pilot PN code from the strongest BS signal.
- Carrier acquisition and tracking of the strongest Pilot. This involves generating the necessary AFC control for the 70MHz local oscillator.
- Clock recovery and tracking to establish synchronisation with the downlink data.
- Provide estimates of the channel coefficients (amplitude, phase and time) for coherent Rake reception of all the other downlink channels.

This functionality is implemented in both dedicated hardware and software, and is discussed in more detail in the following sections.

A. PN Code Acquisition

A simplified block diagram of the Pilot Acquisition circuitry is illustrated in figure 3. This is made up of a mixture of dedicated

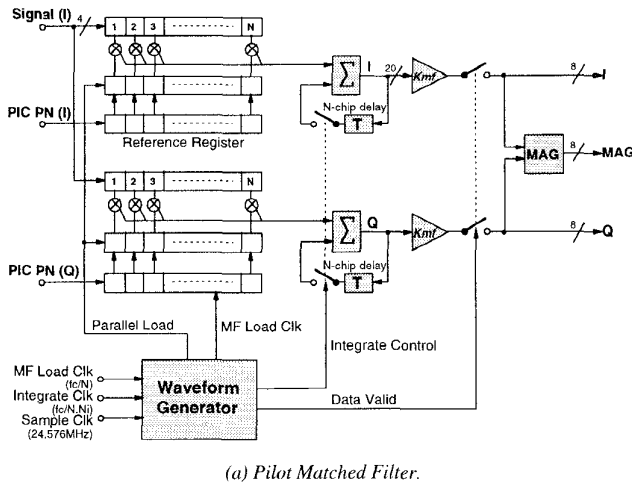
hardware and custom devices, as well as an embedded DSP controller. The main function comprises two matched filters (MF) [6] which generate the complex channel impulse response from the received Pilot signal. This is based upon an FIR filter structure with the length of the impulse response determined by the number of taps in the filter, N . Practical considerations limited this to 128 spreading chips (corresponding to 384 taps with 3 samples per chip) giving an impulse response of 15.6μsec. Initially, the filter weights (the reference Pilot PN sequences) are frozen and the Peak Search function must detect the strongest peak over the complete 16msec period of the PN sequence. The peak is detected from the magnitude (I^2+Q^2) of the MF output and, when a peak is detected above a programmable add-threshold, and it is the strongest, the PN generator is enabled and the integration process initialised. With the wanted BS aligned within the MF correlation window, this extends the effective dynamic range of the correlation process [6]. The initial placement of the correlation peak within the MF is crucial to the whole synchronisation process and is discussed further in section IV.

The number of integrate cycles, N_i , is a critical system parameter since, if it is too high, the resulting complex channel estimates will not follow the rapidly changing phase on each multipath signal. Conversely, if it is too low, the MF dynamic range will be insufficient to allow the resolution of the multipath activity. Clearly there is a compromise here and so this parameter is variable to enable further investigation. The integrate cycle can be varied between 1, 0.5 and 0.25 msec, providing weight update rates of 1, 2 and 4kHz respectively. The actual process of generating the complex channel coefficients is carried out by the Peak Search, Compare and Sort functions, as depicted in figure 3(b). The Peak Search process takes the magnitude, MAG, of the MF output (I^2+Q^2) and searches for peaks in the impulse response. This extends over the length of the matched filter, i.e. a period of 128 spreading chips, corresponding to a time interval of 15.625μsec. As discussed above, the weight update rate has been made programmable in order that it can be optimised for a particular environment. The length of the impulse response was chosen so as to allow the receiver to combine any significant multipath activity in the chosen field trial environments. The results of extensive wideband channel sounding measurements indicate that this period will be sufficient.

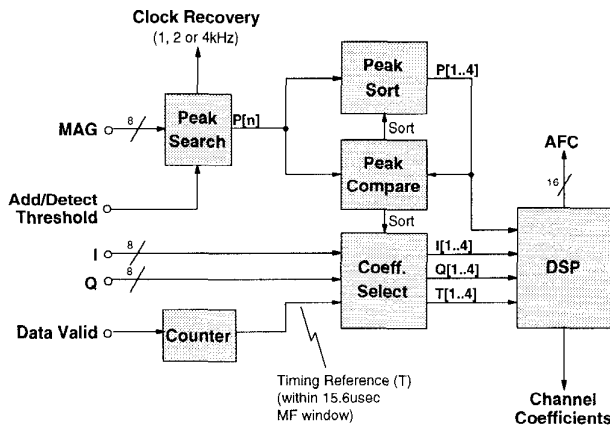
The peaks may be resolved down to a single spreading chip period and it is the task of the Peak Compare and Sort functions to select and order, in terms of signal power, up to four individual multipath components (P[1..4]). The same sorting process is also applied to the I, Q and time (T) information in order to produce the channel coefficients associated with the selected paths. These vectors (P, I, Q and T) are passed to the embedded DSP which produces the necessary complex weights and time delays for the Rake receiver. The I and Q values enable co-phasing of the individual multipath components whilst normalising the power of each path to the strongest, i.e. ensuring maximal ratio combining.

Since both BS's employ the same pilot PN sequence but with a known offset, another MF structure is employed to search for the second BS pilot. If a call isn't in progress, and a new BS pilot signal is detected above the present one, then the receiver resets itself and locks to the new BS. However, if a call is active, a handover is then initiated to the second BS.

In terms of the hardware implementation a compromise had to be made between providing a flexible architecture on the one hand and maintaining performance objectives on the other. This was achieved by exploiting some readily available custom high speed digital devices, e.g. the HSP45256 binary correlator for the Pilot matched filter, along with FPGA technology (Xilinx XC4000 devices) for the Pilot detect functions. The FPGA technology ensures that the multipath activity can be detected and sorted in real-time, whilst the DSP provides some degree of flexibility in the way in which the coefficients are generated and the Rake programmed. The chosen DSP platform was the Texas Instruments C40 processor which performs the final selection of the channel coefficients before programming the Rake receiver. The DSP also controls the whole synchronisation process as well as implementing the handover protocol and maintaining communications with the higher layers in the protocol stack.



(a) Pilot Matched Filter.



(b) Pilot Detect.

Figure 3: Pilot Acquisition & Tracking functions.

B. Carrier Acquisition & Tracking

Carrier acquisition and tracking is performed using the complex (I/Q) outputs from the pilot matched filter, specifically by determining the rate of change of phase (and thereby frequency

error) in the DSP block, as shown in figure 3(b). A 16-bit error control signal is provided by the DSP to enable automatic frequency control (AFC) to be implemented, and the loop filter of a digital phase/frequency-locked loop is also embedded within the DSP.

The basis exists for a completely digital receiver, using an A/D converter in the last IF stage, the error signal programming a numerically controlled oscillator, and final downconversion being carried out in a digital complex multiplier [7]. This method is one option being investigated for the LINK system demonstrator, although the initial design uses a direct digital frequency synthesiser generating 70MHz as the automatic frequency controlled local oscillator, with the quadrature downconversion being carried out by analogue means. The resultant I and Q baseband signals are digitised in a dual A/D converter before being sent to the matched filters.

C. Clock Recovery & Tracking

All receiver clocks are derived from the pilot matched filter, which provides a reference signal to an analogue phase-locked loop (PLL). The reference consists of a square wave obtained from the MF magnitude measurement ($I^2 + Q^2$), as shown in figure 3, and is at 1, 2 or 4kHz depending on the chosen length of the filter correlation window. The PLL tracking circuit generates the system clock running at 24.576MHz, and the feedback signal to the phase detector and all the other required clocks are then derived by dividing down: the PRBS chipping clock at 8.192MHz, data and bearer clocks at 64 and 128kHz, power control channel and pilot clocks (0.25 to 4kHz), and interleaver frame clocks at 83.3 and 27.8Hz.

The raw outputs from the divider chain are synchronised to give precise edge alignment, and buffered prior to distribution to the other blocks within the receiver. The clock and PRBS generators are combined on a separate circuit board. A particularly critical part of the synchronisation process is to ensure that the feedback signal from the divider chain to the PLL phase detector is correctly positioned within the MF correlation window. This provides robust tracking of the MF correlation peak (PLL reference), and is achieved by incorporating a programmable delay block between the divider chain output and the phase detector input.

IV. SYSTEM ACQUISITION

Once the Pilot has been acquired and is being tracked and the complex channel estimates are available, the SYC channel must be despread, decoded and the system information extracted by the MS Controller. The SYC channel comprises a fixed length message at a rate of 1kbps. There are 144 message bits giving an overall Sync frame period of 144msec, or 9 complete Pilot periods as shown in figure 4(a). Amongst other general system information (BS ID, Tx power, etc.), the message contains the state of the long PN code generator at the BS. This state is valid at the next Sync Frame boundary and allows the MS to preset its own long code generator so that, at the prescribed reference time, the generator can be enabled. The MS can then receive any paging message on the FCC for the case of a network-originated call or, alternatively, initiate a call on the uplink. This process is illustrated in figure 4(b). Note, that no specific paging channel has been allocated, i.e. another common system channel, since with each user identified by its own

unique offset of the long PN code, the FCC channel can be employed.

In order to extract the necessary system information from the SYC channel, symbol synchronisation must be established initially. This is derived from the Pilot acquisition and tracking process which aligns the reference Pilot signal and the incoming Pilot in the matched filter at a reference offset of the code. The clock generation process then aligns all the symbol clocks with the Pilot PN reference (every 16msec) and establishes symbol synchronisation. The SYC channel can then be despread to determine the Sync framing and, consequently, frame synchronisation. This is shown in the frame structure of figure 4(a), with the 12 or 36msec traffic frames aligned within the 144msec Sync frame.

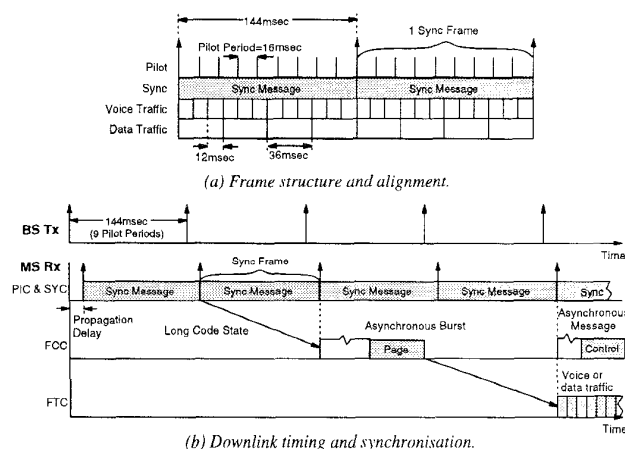


Figure 4: System timing and framing.

V. DISCUSSION

The LINK CDMA project is now very much in the development phase, with full system integration planned for mid 1995. The aim is to carry out extensive field trials in the Bristol area and to present the results to as large a forum as possible. The hope is to be able to influence to some extent the work within ETSI in the selection of the air interface for UMTS, as well as to improve the general understanding of a CDMA system and the many problems it presents to system and network designers. This contribution has only touched briefly on one of the many complex issues relating to the successful operation of a complete DS-CDMA system and it is hoped that further publications on this, and other key system issues, will be forthcoming as the field trials progress.

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